Reg.No. _____

Karunya UNIVERSITY

(Karunya Institute of Technology & Sciences)

(Declared as Deemed-to-be University under Sec.3 of the UGC Act, 1956)

End Semester Examination – Nov/Dec – 2016

Code : 14EC3019

Sub. Name : Digital System and ASIC Design

Semester : 2016-17 ODD

Duration : 3hrs

Max. marks : 100

ANSWER ALL QUESTIONS (5 x 20 = 100 Marks)

Q. No.	Sub Div.	Questions	Course Outcome	Marks
1.	a.	Implement the following Boolean functions using the PAL device. W(A, B, C, D) = Σm(2, 12, 13) X(A, B, C, D) = Σm(7, 8, 9, 10, 11, 12, 13, 14, 15) Y(A, B, C, D) = Σm(0, 2, 3, 4, 5, 6, 7, 8, 10, 11, 15) Z(A, B, C, D) = Σm(1, 2, 8, 12, 13)	CO1	**10**
	b.	Draw the ASM chart for a mod -8 binary up- down counter	CO1	**6**
	c.	Compare Mealy machine and Moore machine	CO1	**4**
		(OR)		
2.	a.	Design a Asynchronous sequential circuit with two inputs x1 and x2 and one output Z. Initially, both inputs are equal to zero. When x1 or x2 becomes '1', the output Z becomes 1. When the second input also becomes 1, the output changes to 0. The output stays at 0 until the circuit goes back to the intial state. Draw the Asynchronous sequential logic circuit using D flipflop	CO1	**12**
	b.	Explain the different types of Hazards?	CO1	**3**
	c.	Implement a Full adder circuit with a decoder and two OR gates S(x,y,z) = Σm (1,2,4,7) C(x,y,z) = Σm (3,5,6,7)	CO1	**5**
3.	a.	Design a Sequence Detector that produces output '1' using Mealy machine whenever the overlapping sequence 101101 is detected using ASM chart.Draw the Synchronous sequential logic circuit for the same using JK flipflop	CO1	**12**
	b.	Draw the PLA realization for the above circuit(Sequence Detector)	CO1	**6**
	c.	Mention the advantages of PLD.	CO1	**2**
		(OR)		
4.	a.	What is Programmable ASIC? Mention the different programming technologies used in Programmable ASIC.	CO2	**3**
	b.	Explain the Xilinx XC 4000 family IOB architecture with neat diagram. And also explain the Xilinx LCA timing model with diagrams.	CO3	**12**
	c.	Explain the problems that occur in the Asynchronous Sequential circuits while designing?	CO1	**5**
5.	a.	List out the different types of ASIC? Explain briefly about Semi custom ASIC?	CO2	**13**
	b.	Draw the Altera FLEX architecture (Logic array Block) and explain its working?	CO3	**7**
		(OR)		
6.	a.	Explain the Altera MAX architecture (Logic array Block) with neat diagram. And also explain the Altera MAX timing model with diagrams.	CO3	**10**

	b.	Draw the Physical Design flow and briefly explain the process flow with the significance of each stage in the design flow?	CO2	**10**
7.	a.	Explain the Xilinx LCA interconnect architecture with neat diagram?	CO3	**12**
	b.	List out the differences between the CPLD and FPGA.	CO3	**2**
	c.	Draw the Altera MAX 9000 interconnect scheme and explain it's working	CO3	**6**
		(OR)		
8.	a.	Draw the Xilinx FPGA Design flow and briefly explain the process flow with the significance of each stage in the design flow?	CO2	**8**
	b.	Explain the format of the input and output files used by the PLA design tool expresso.	CO2	**4**
	c.	Explain hierarchical nature of an EDIF (Electronic Design Interchange Format) file.	CO2	**6**
	d.	What is meant by Half gate ASIC?	CO2	**2**
		Compulsory:		
9.	a.	Explain Xilinx Spartan II Configurable logic block in detail.	CO3	**8**
	b.	Design BCD counter using CPLD structure. (Use D flipflop)	CO3	**12**

ALL THE BEST